

The diagram illustrates a display system architecture. A **TIMING CONTROLLER** (2) is connected to a **DISPLAY PART** (6). The **DISPLAY PART** is divided into two main sections: a vertical column of four blocks (3) and a horizontal row of four blocks (M1, M2, M9, M10). The Timing Controller (2) is connected to the vertical column (3) and the horizontal row (M1, M2, M9, M10). The horizontal row is also connected to a block (4) which is connected to the vertical column (3).

FIG. 2A

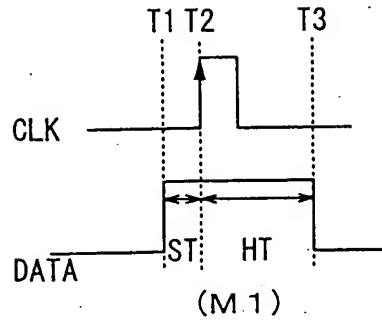


FIG. 2B

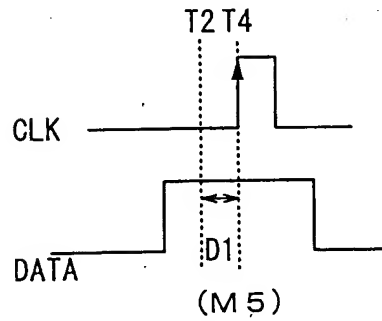
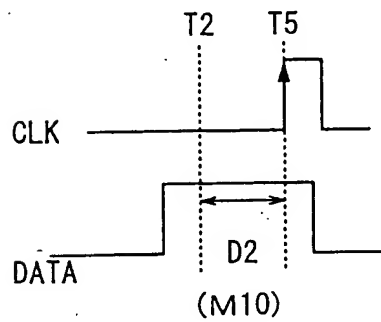


FIG. 2C



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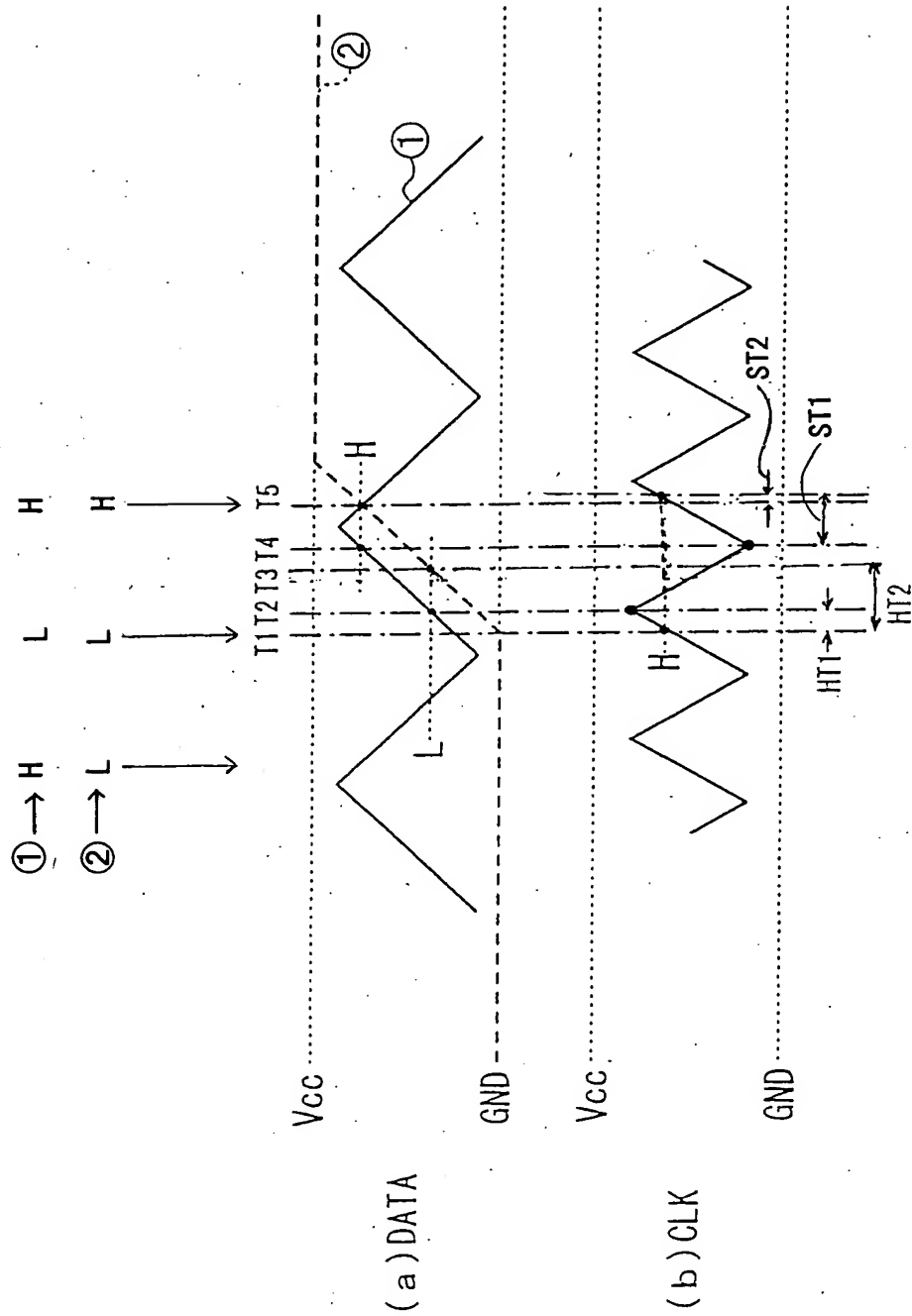
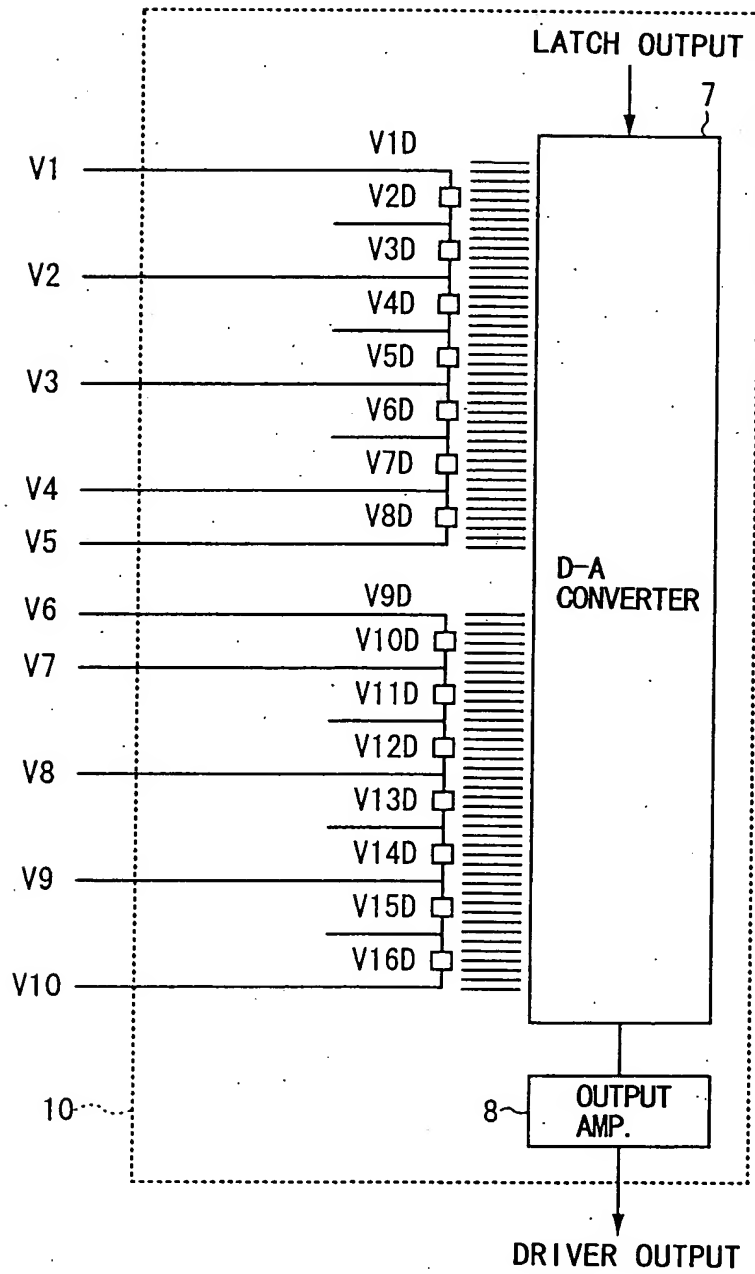


FIG. 3

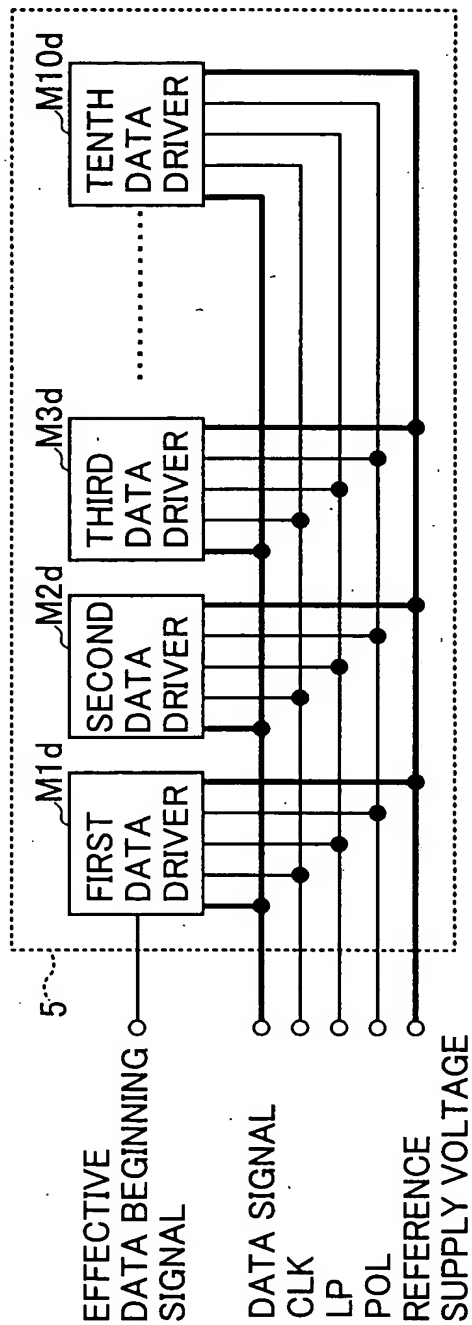
FIG. 4



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FIG.5



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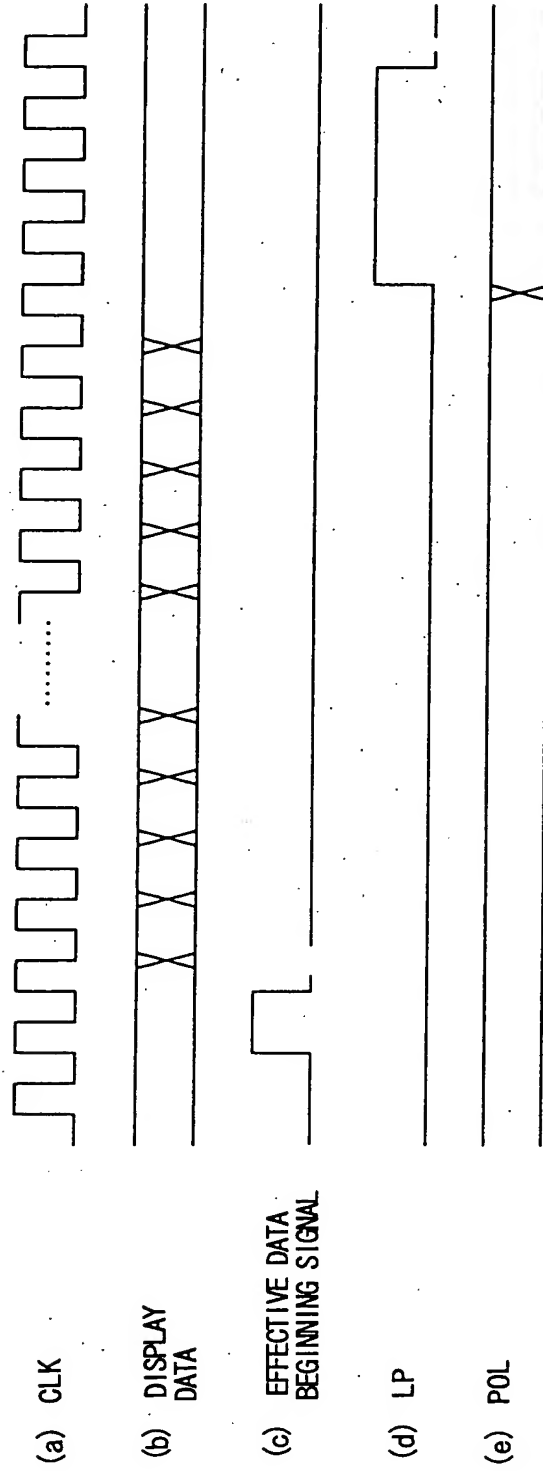


FIG. 6

FIG. 7

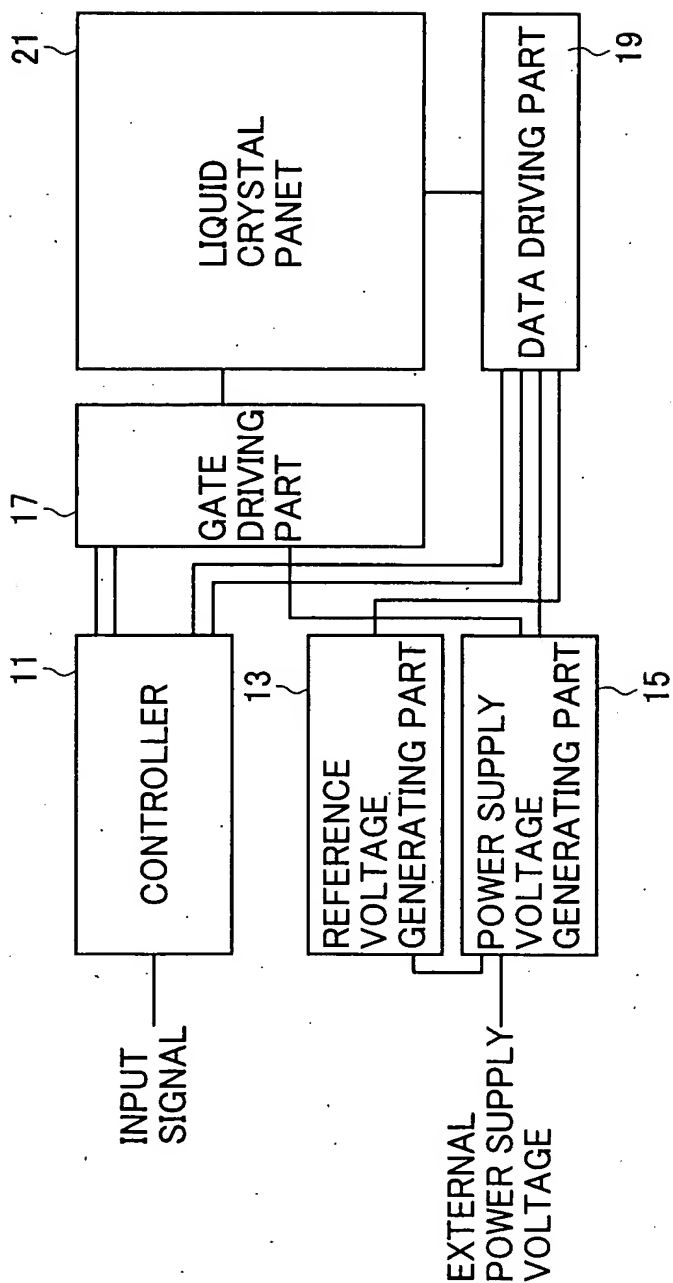


FIG.8

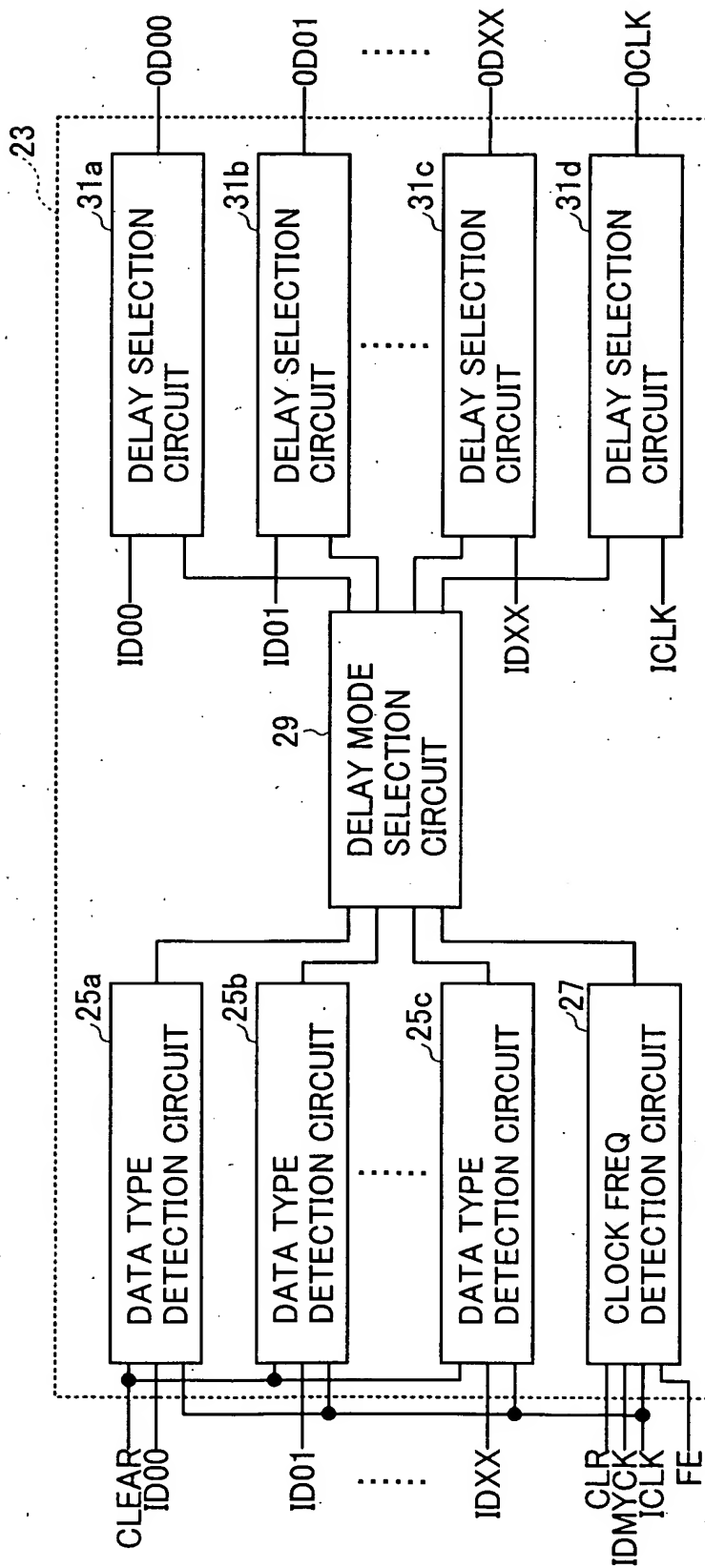


FIG. 9

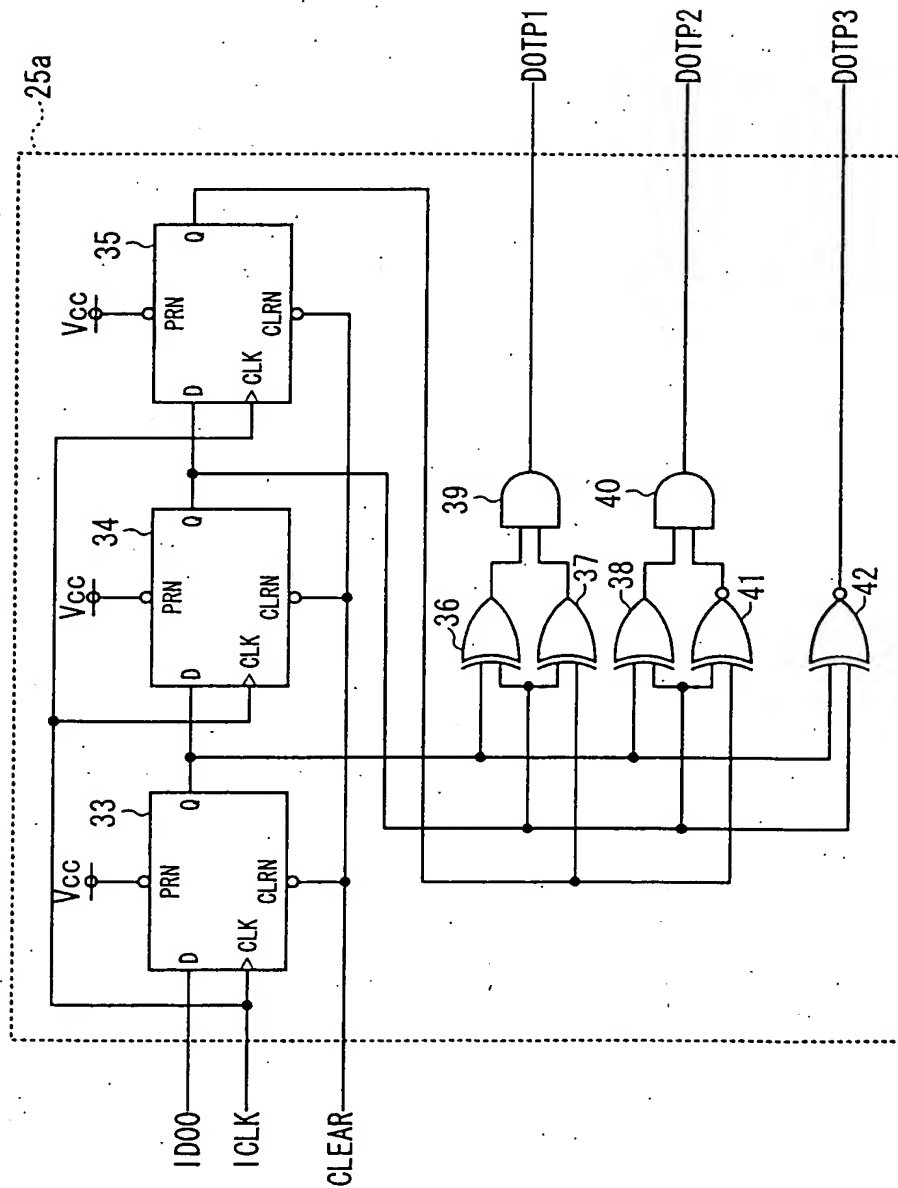


FIG. 10

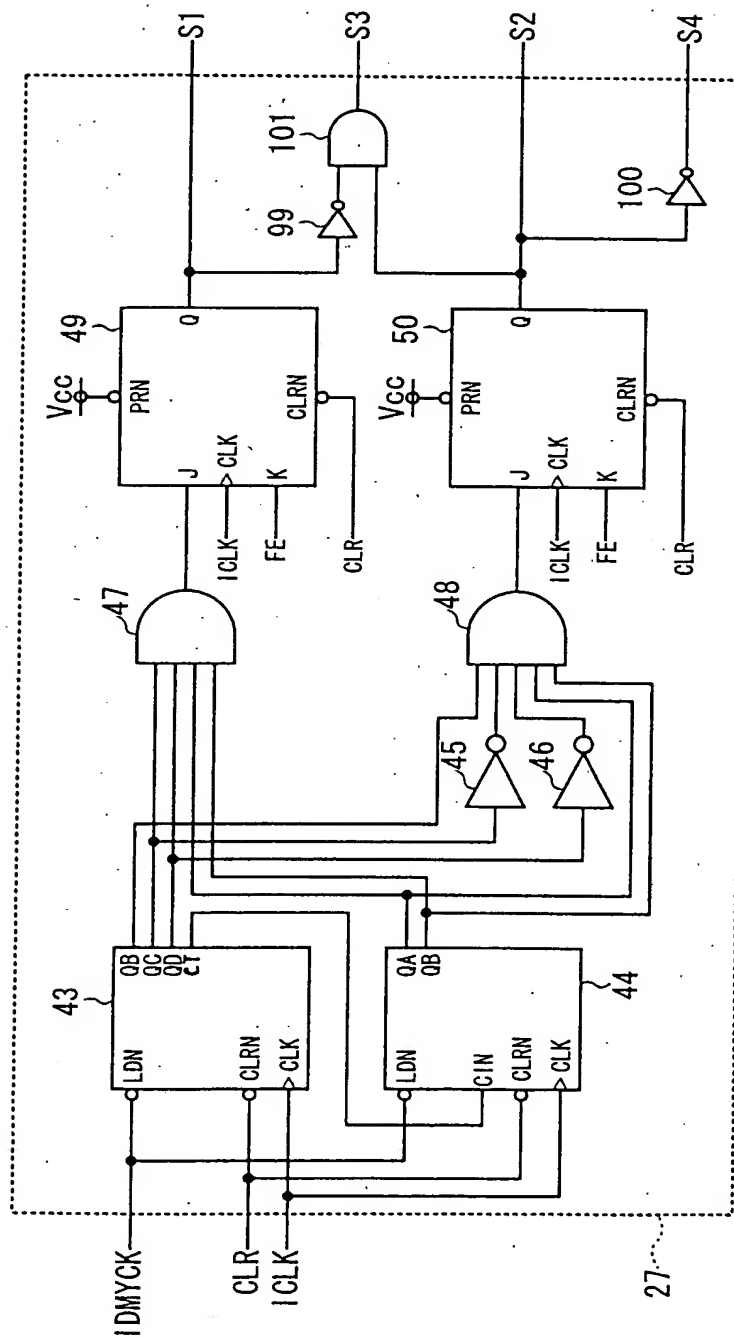


FIG. 11

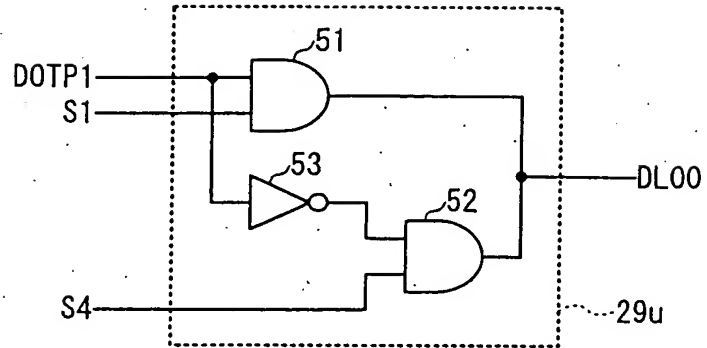
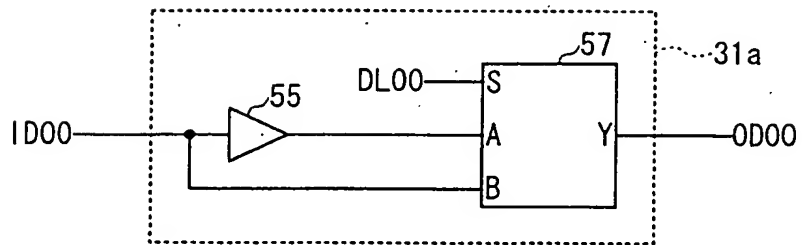


FIG. 12



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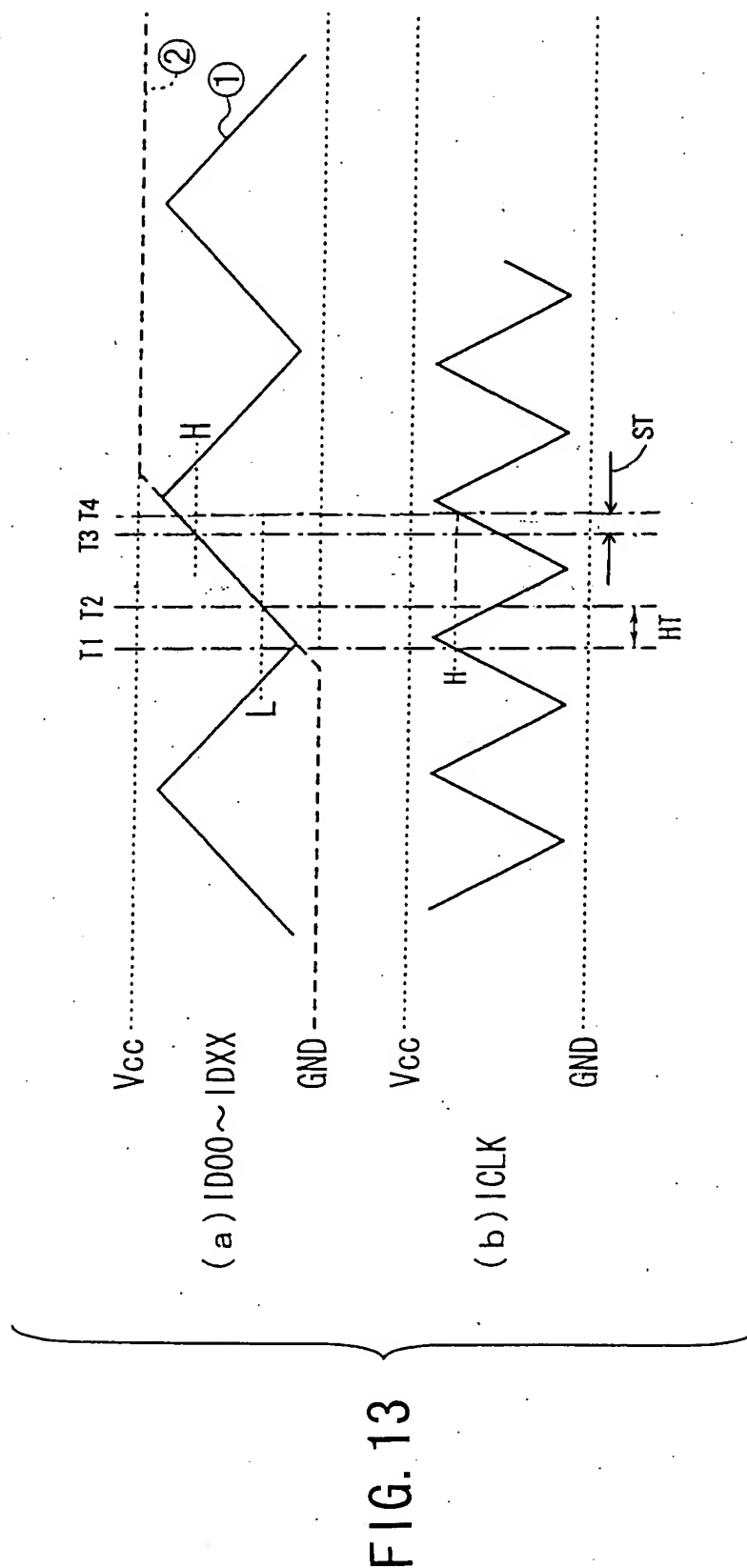


FIG. 14A

(COLUMN)

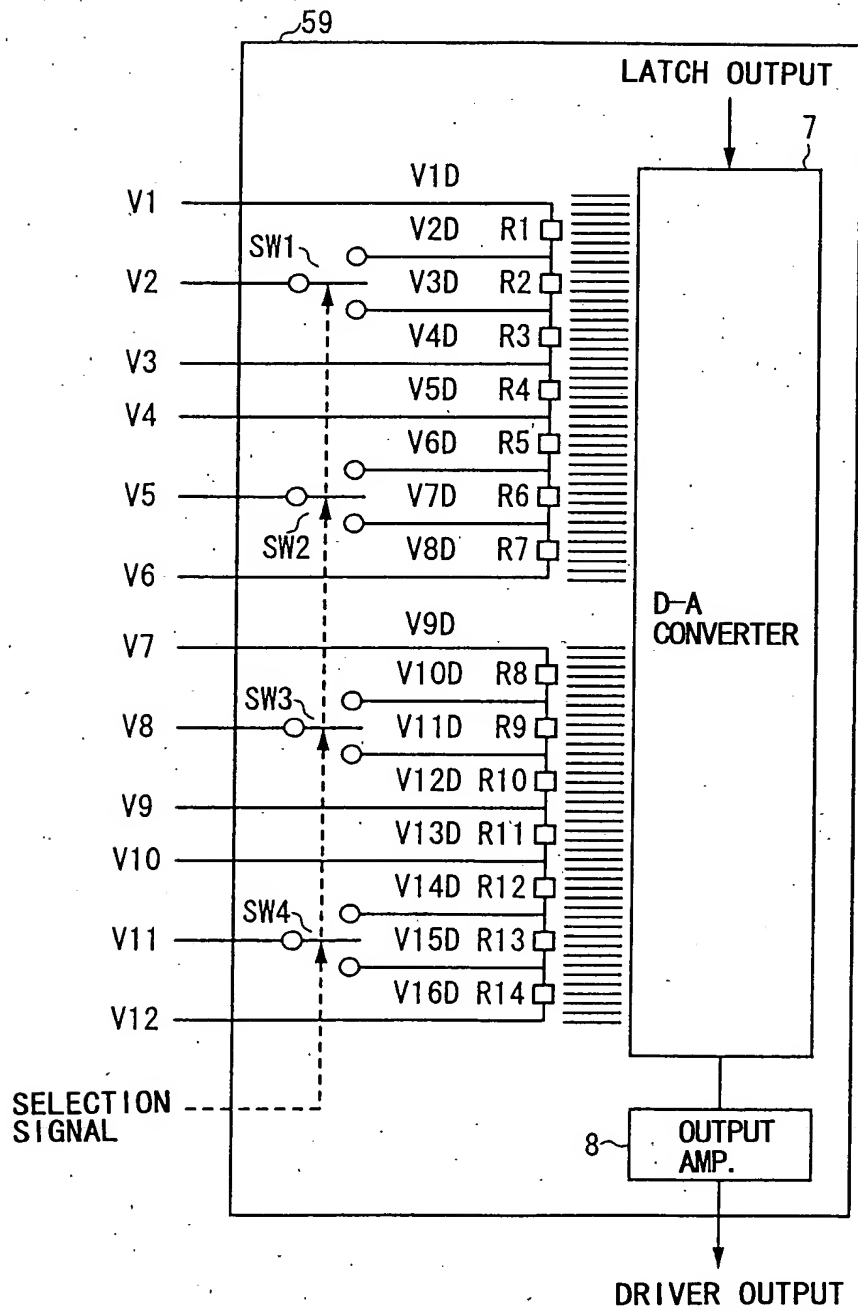
	1ST	2ND	3RD	4TH	5TH
	RGB	RGB	RGB	RGB	RGB
(LINE) 1ST	■	■			■
2ND	■	■			■
3RD	■	■			■
4TH	■	■			■
5TH	■	■			■

FIG. 14B

	1ST	2ND	3RD	4TH	5TH
	RGB	RGB	RGB	RGB	RGB
1ST	■	■			■
2ND	■	■			■
3RD			■	■	
4TH			■	■	
5TH	■	■			■

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FIG. 15



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FIG. 16A

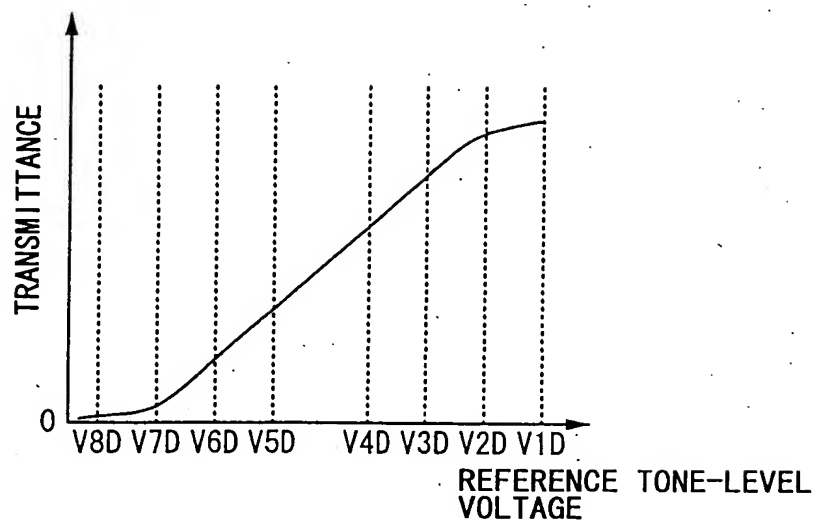
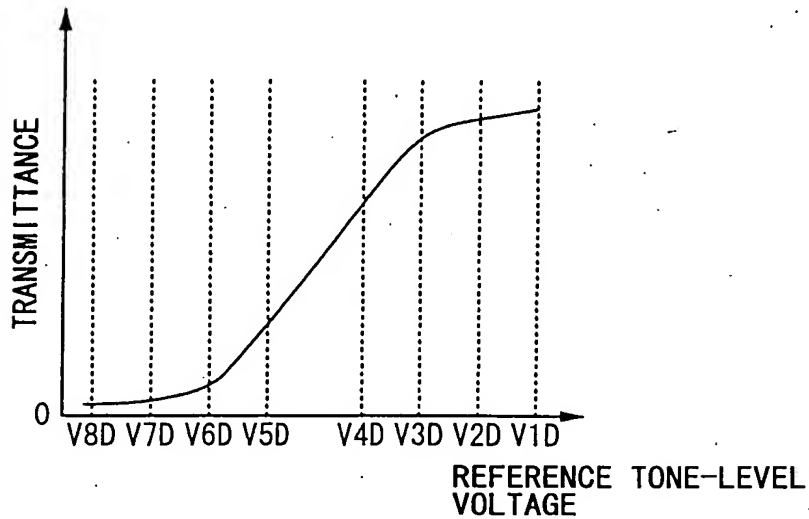


FIG. 16B



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FIG.17

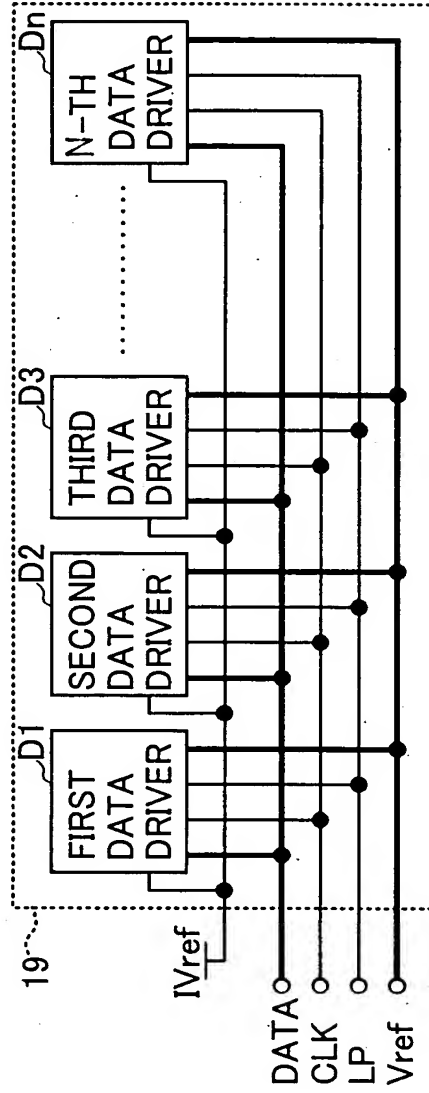
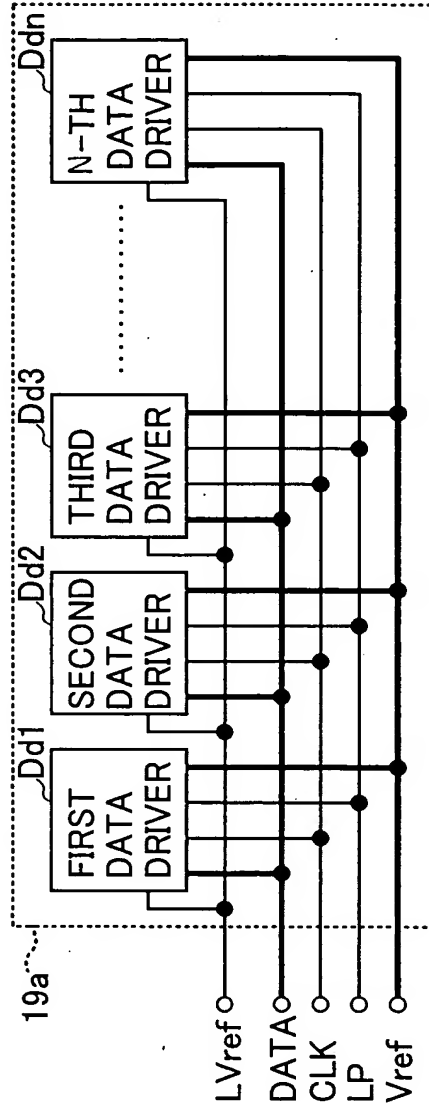
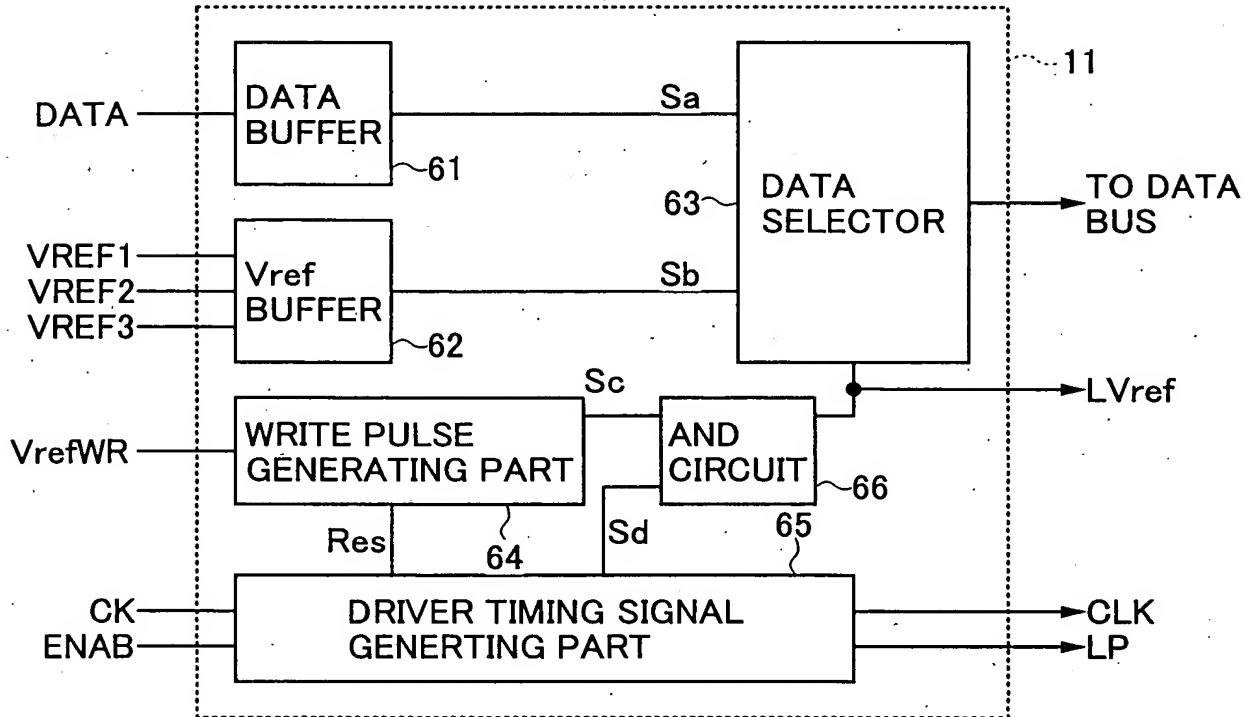


FIG.18



FOOTNOTES

FIG.19



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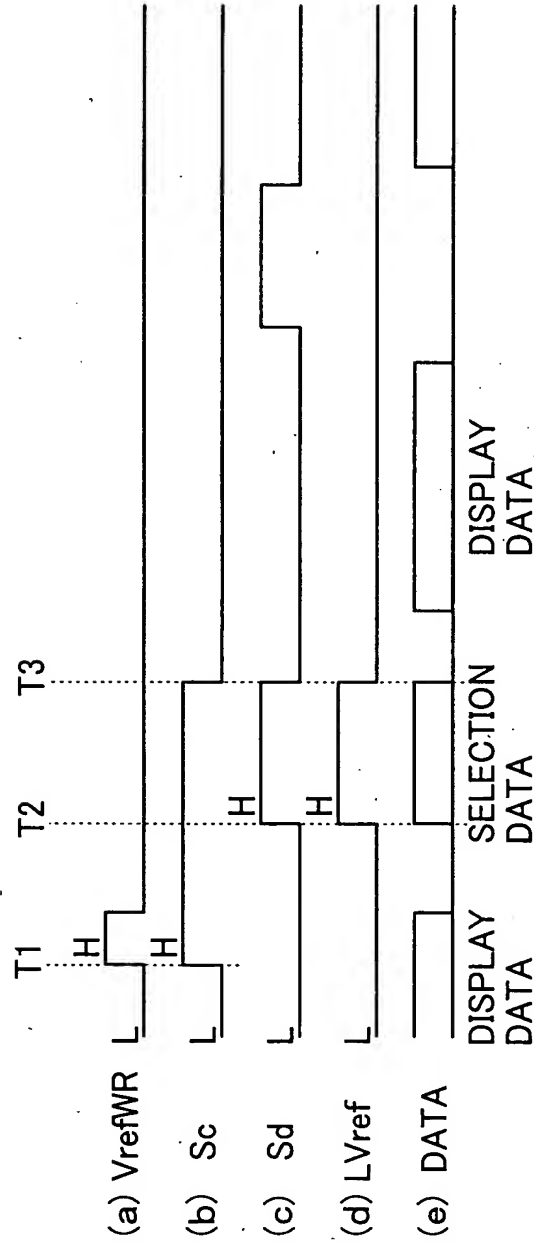
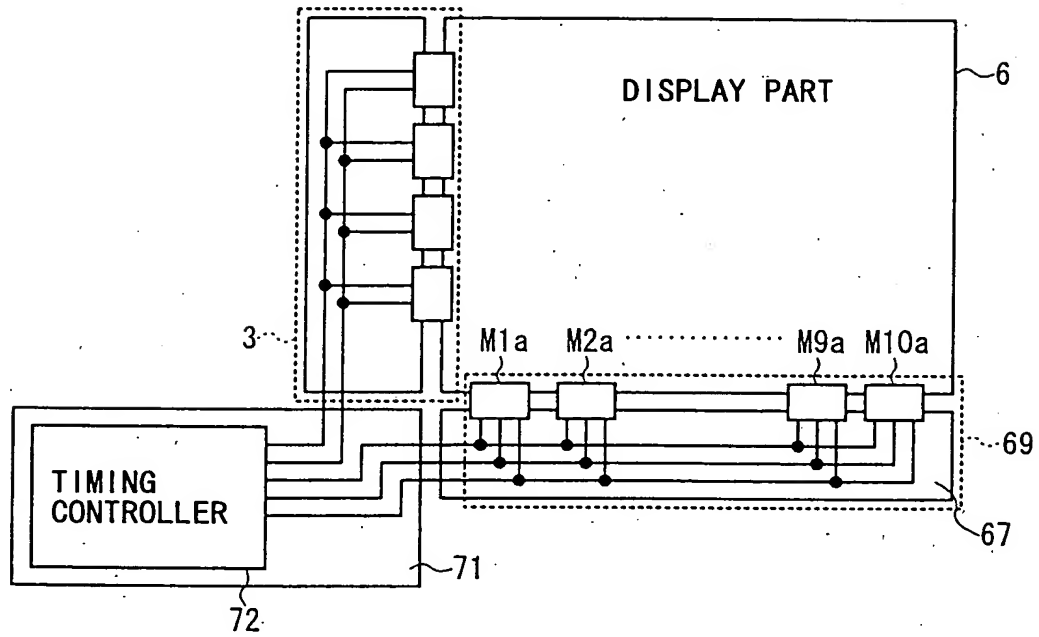


FIG.20

FIG. 21



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FIG. 22A

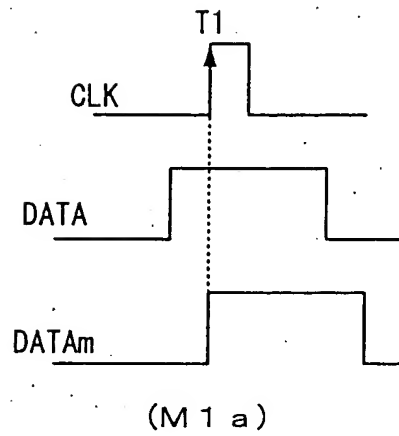
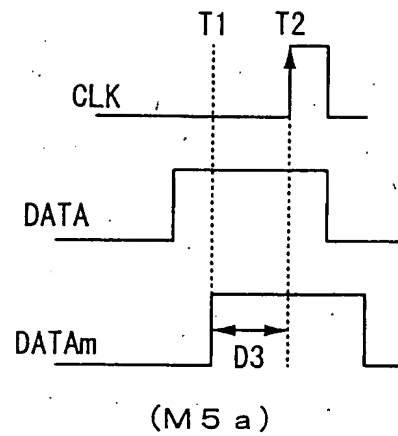


FIG. 22B



101121 5905001

FIG. 23

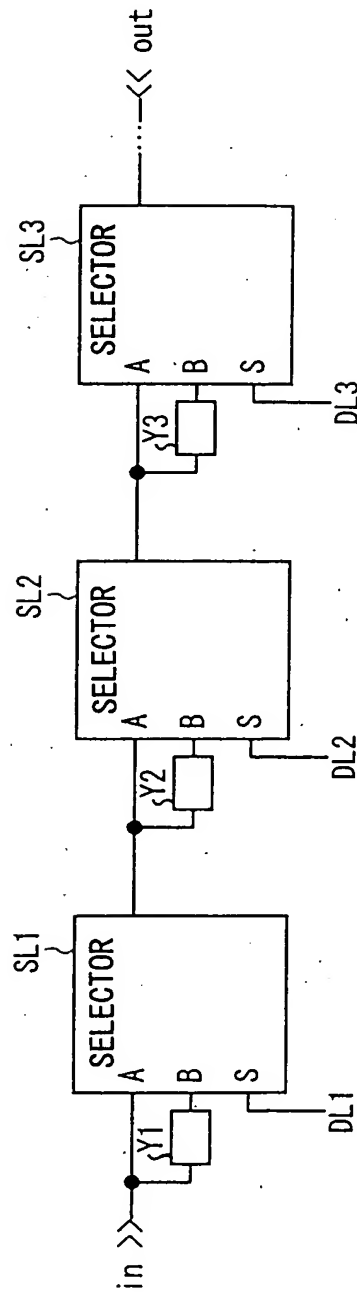
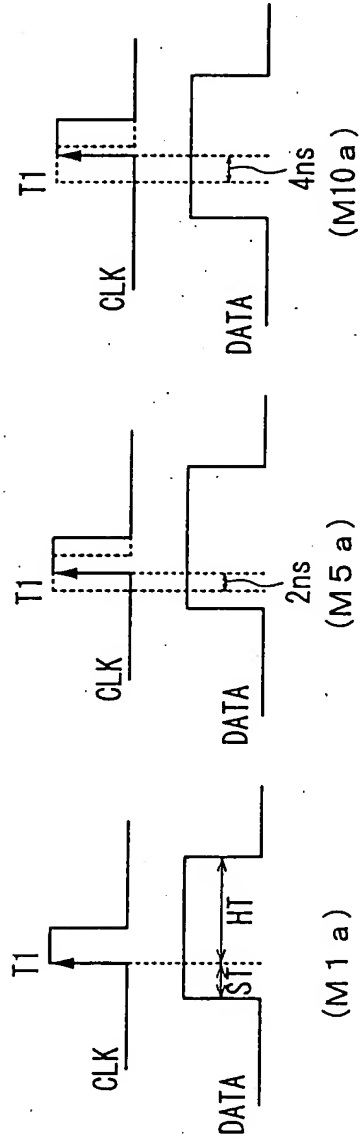


FIG. 24A FIG. 24B FIG. 24C



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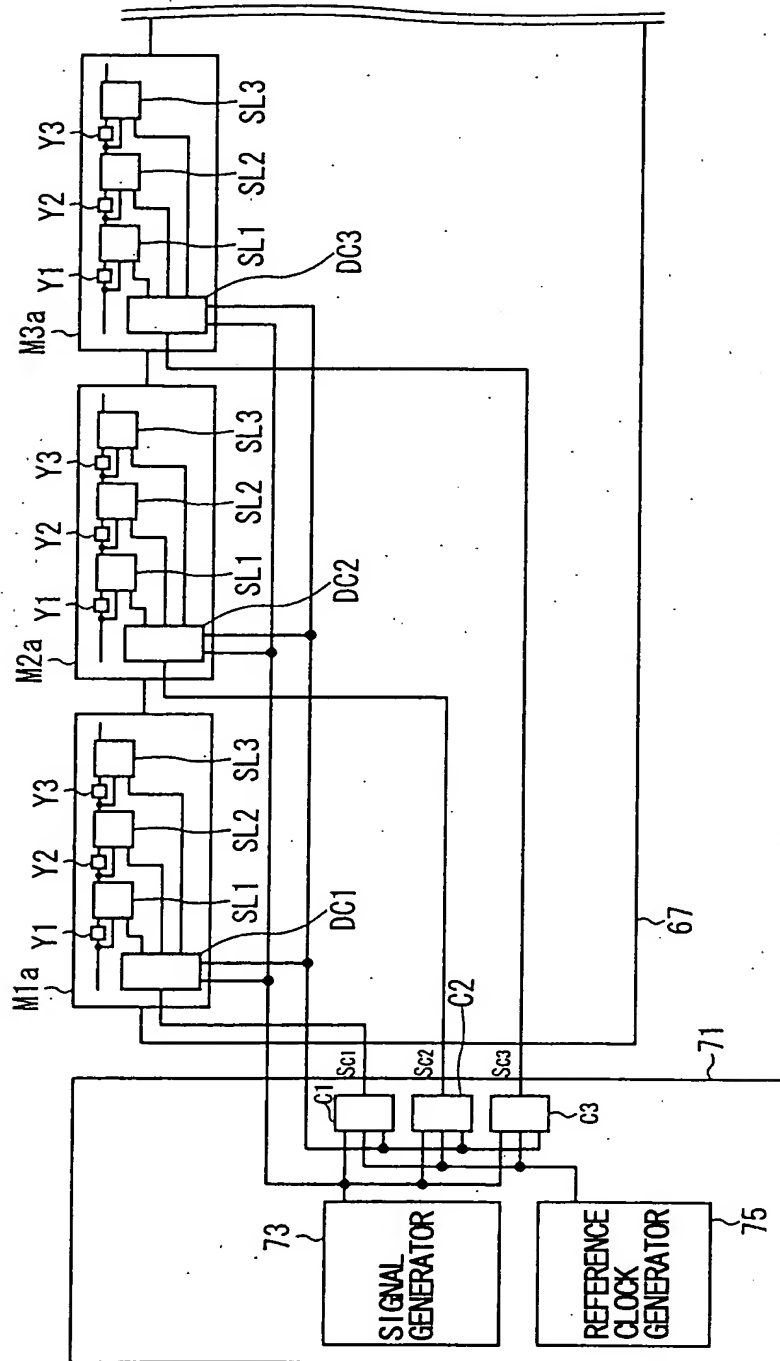
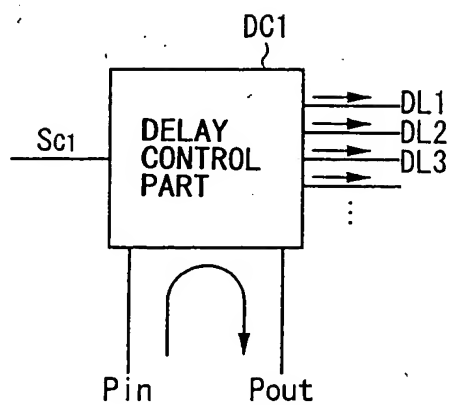
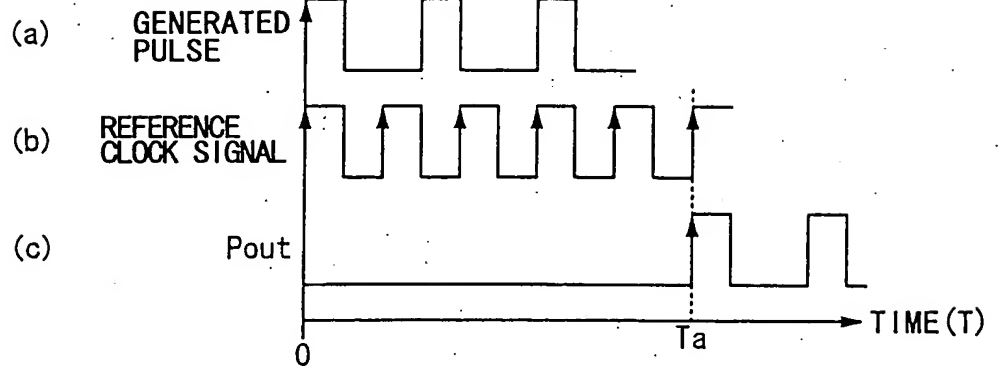


FIG. 26



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101121" 5951001

FIG. 27



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FIG. 28

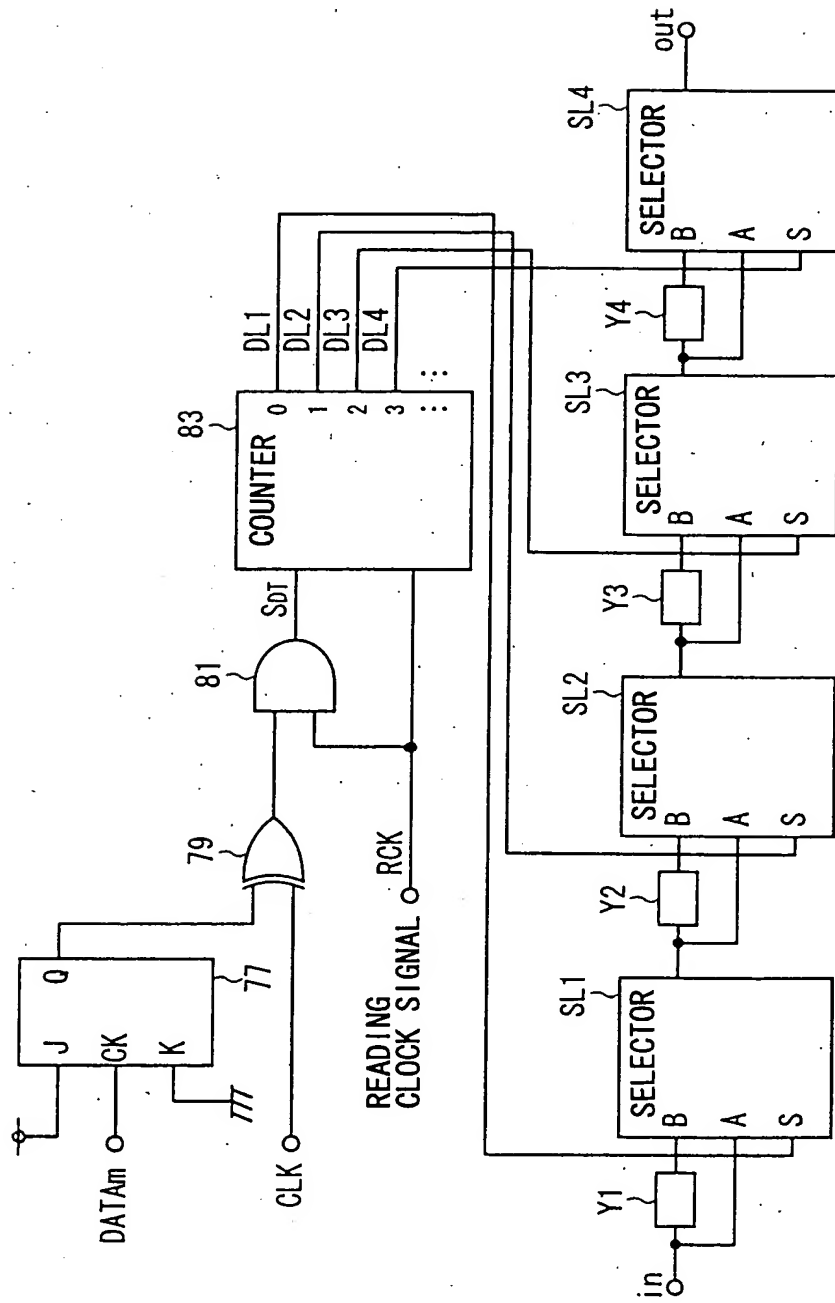


FIG. 29A

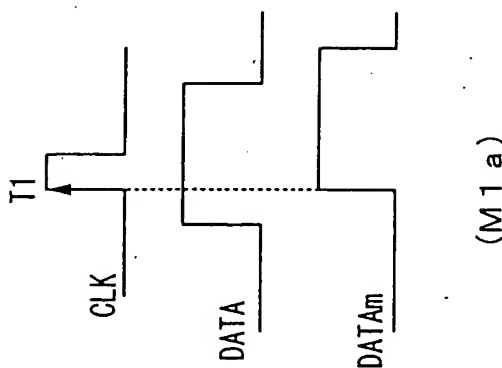


FIG. 29B

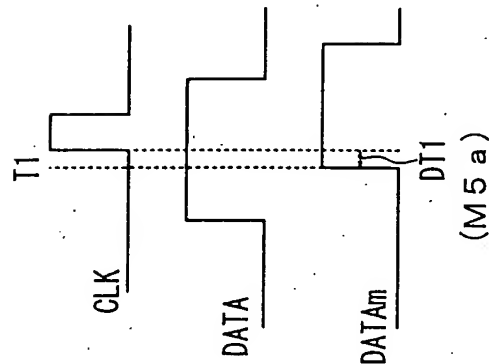
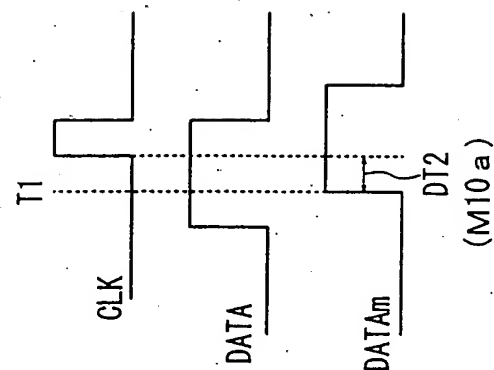


FIG. 29C



1005055 1001

FIG.30

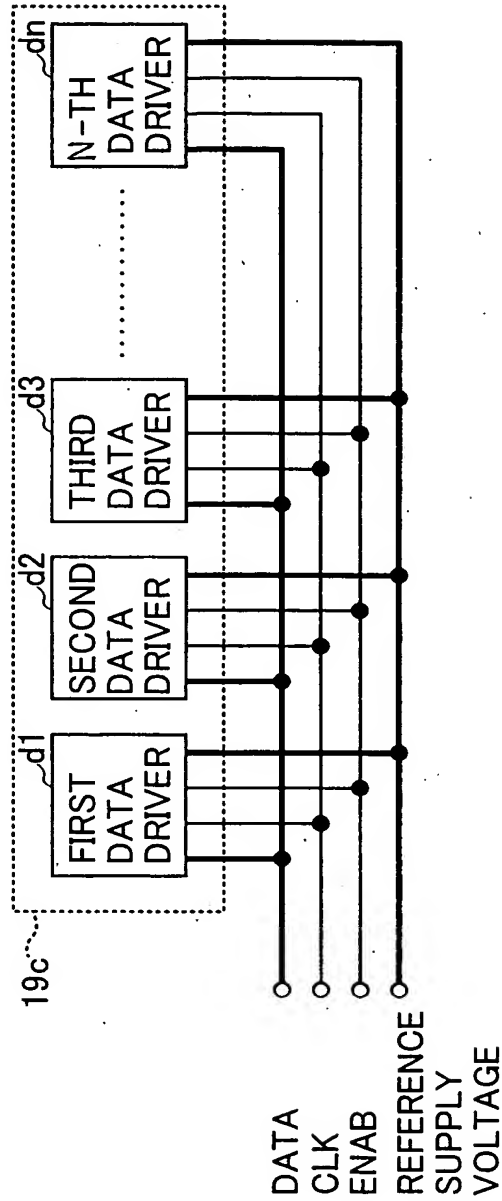


FIG. 31

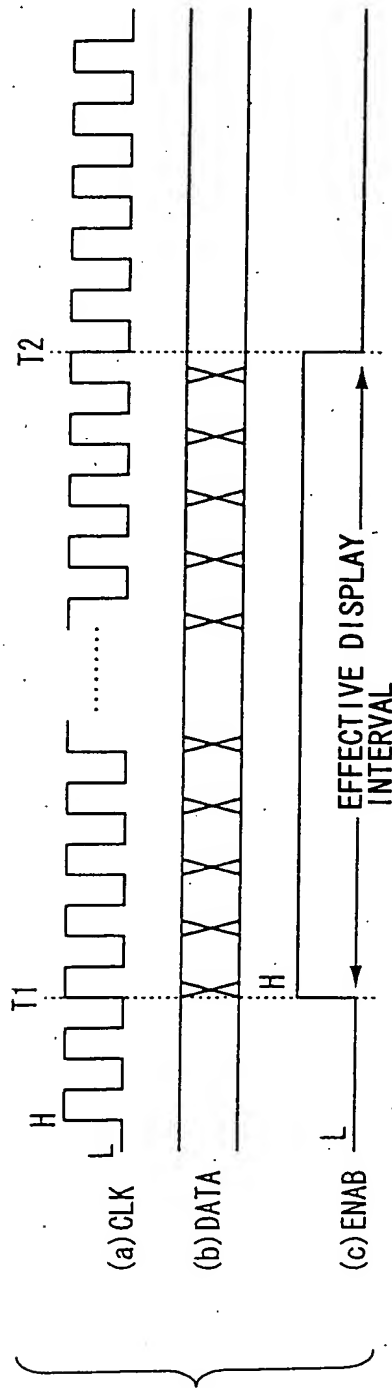


FIG. 31

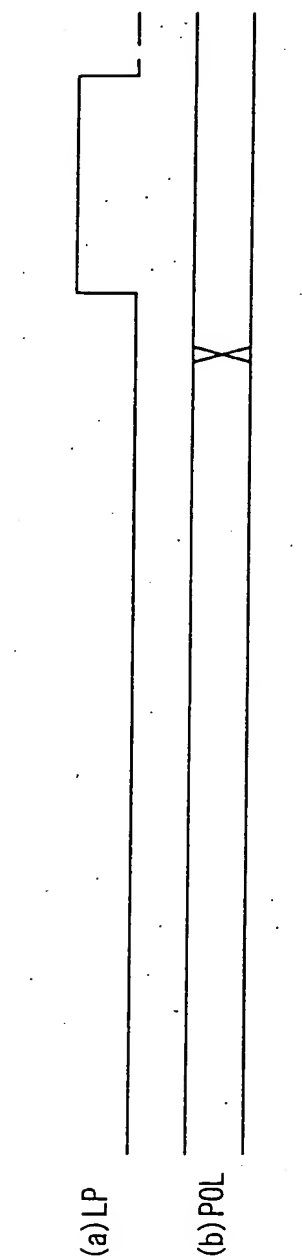


FIG. 32

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FIG.33

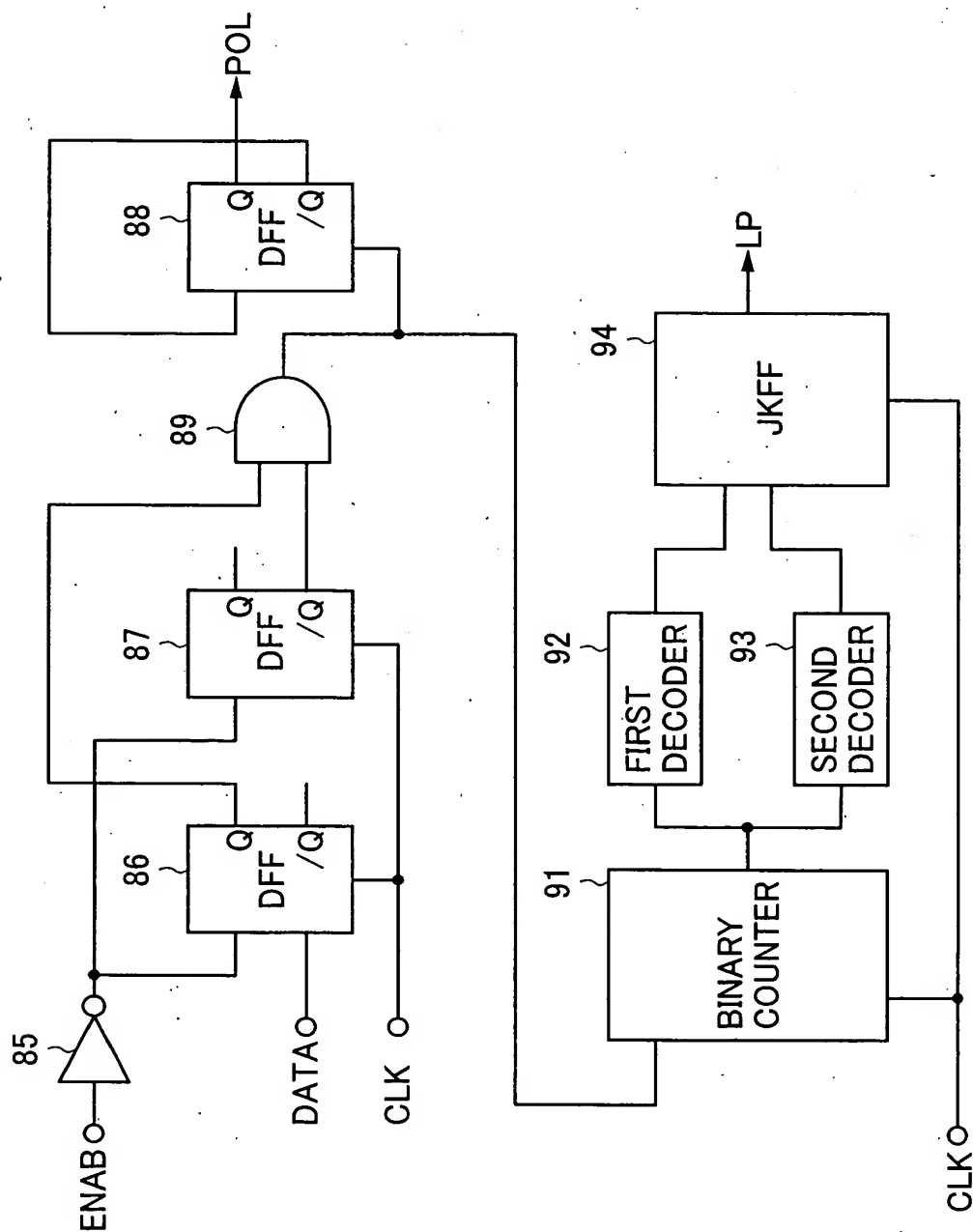


FIG. 34

